Hall Ticket Number:

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Code No.: 22601 M

VASAVI COLLEGE OF ENGINEERING (Autonomous), HYDERABAD
M.E. (ECE: CBCS) II-Semester Make Up Examinations, September-2017
(Embedded Systems & VLSI Design)

Mixed Signal IC Design

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from Part-B*

Part-A (10 × 2 = 20 Marks)

1. Explain how analog and digital circuits, fabricated on the same substrate function.
2. What is Phase Locked Loop?
3. How is an integrated capacitor of a switched capacitor circuit fabricated?
4. Explain the specialty of latched comparator.
5. Draw the track mode sample-hold circuit using switching capacitor.
6. What is the effect of charge injection that occurs in open-loop sample-hold circuit?
7. How quantization noise behavior in A/D converter is estimated using deterministic approach?
8. What is the advantage of hybrid D/A converter?
9. A band-limited signal has a frequency of 49 Hz and sample frequency is 100 Hz. Calculate Oversampling Ratio (OSR)?
10. What is the role of phase detector of a phase-locked loop?

Part-B (5 × 10 = 50 Marks)

11. a) Indicate the drawbacks of Delay Locked Loop (DLL). [5]
    b) State the problems of covering both analog and digital circuits on the same substrate. [5]
12. a) Explain the complete analysis of parasitic insensitive integrator circuit using switched capacitor circuit. [6]
    b) Explain BiCMOS comparator. [4]
13. a) Draw and explain sample-hold circuit using diode-bridge. [5]
    b) A 12-bit A/D converter has a reference voltage V_{ref} = 2V. Find rms value of the quantization noise. [5]
14. a) Consider a 2-bit thermometer based D/A converter. Calculate the analog output voltage (V_{out}) obtained for different combinations of the input bits if V_{ref} = 5 V and the full scale gain of the opamp is 1. [5]
    b) Explain four-bit folding A/D converter. [5]
15. a) Explain the charge pump phase detector. [5]
    b) Explain delta sigma A/D converter. [5]
16. a) How do you use PLL to eliminate the skew? [5]
    b) Draw and explain switched capacitor low-Q Bi-quad filter. [5]
17. Answer any ***two*** of the following:
    a) Switched capacitor based sample-hold circuit. [5]
    b) Interpolating A/D converter. [5]
    c) Given that a 1-bit A/D converter has a 6-dB SQNR, what sample rate is required to obtain a 72 dB (or 12 bits) if f_0 = 50 KHz for straight oversampling as well as first-and second-order noise shaping? [5]